

REMARKS

Claims 1, 2, 4, 6 and 7 currently remain in the application. Claims 3, 5, 8 and 9 have been withdrawn as non-elected claims. Claim 1 has earlier been amended.

Claims 1, 2, 4, 6 and 7 were rejected under 35 U.S.C. 103 over Matsui in view of Tate. The Examiner seems to be of the opinion that Matsui fails to predicate the rejection of these claims on the anticipation ground only because there is no disclosure of a plurality of terminal-forming areas that are no greater than corresponding one of the electronic components and a plurality of specified terminal-forming areas including a plurality of terminal parts directly thereon such that each pair of the terminal parts within any one of the terminal-forming areas is closer to each other than any pair of the terminal parts in different ones of the terminal-forming areas (lines 5-9 of Paragraph 3 of the Official Letter). Thus, the Examiner additionally cited Tate and concluded that it would have been obvious to modify Matsui according to the teaching of Tate.

This, however, is not the only inventive element of the rejected claims that was not disclosed by Matsui. Matsui discloses no more than the use of an isotropic conductive film for the connection of one electronic element (such as LSI chip), and this is not an important aspect of the present invention, as should be clear from the Background of the Invention section of the specification. What Matsui additionally fails to disclose is the step of forming "an anisotropic conductive layer on a target surface so as to span a plurality of terminal-forming areas" where the plurality of these terminal-forming areas are specified areas on which a plurality of electronic components are surface-mounted. In the above, "an anisotropic conductive layer" means "one single anisotropic conductive layer". Matsui does not disclose any single anisotropic conductive layer large enough to span a plurality of terminal forming areas on which a plurality of electronic devices are surface-mounted.

Tate discloses conductive adhesive elements provided corresponding to individual ones of a plurality of electronic devices and fails to disclose or even hint at a large enough isotropic conductive film (such as shown at 5 in Fig. 4) for spanning over a plurality of electronic devices (such as shown at D1, D2 and D3 in Fig. 4) through a plurality of terminal-forming areas (such as 3a, 3b and 3c shown in Fig. 4).

Thus, it should be concluded that these two references, even if considered in

combination, cannot predicate the Examiner's rejection. Moreover, it must be admitted that the positioning of the terminals of the plurality of electronic devices with respect to the terminal-forming areas becomes difficult according to this invention in spite of the advantages to be gained thereby. This also leads one to believe that ordinary persons skilled in the art would not find it difficult to conceive the instant inventive elements even in light of these cited references.

In summary, it is believed that the application is now in condition for allowance.

Respectfully submitted,


Keiichi Nishimura
Registration No. 29,093



October 1, 2003
BEYER WEAVER & THOMAS, LLP
P.O. Box 778
Berkeley, CA 94704-0778
Telephone: (510) 843-6200
Telefax: (510) 843-6203